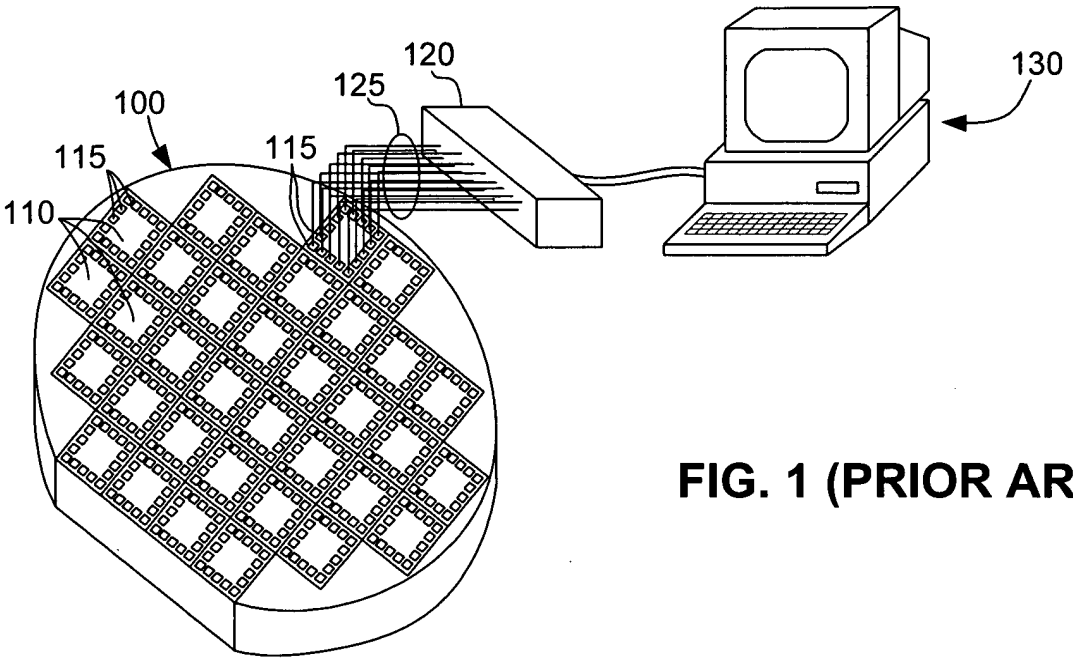

FIG. 1 (PRIOR ART)

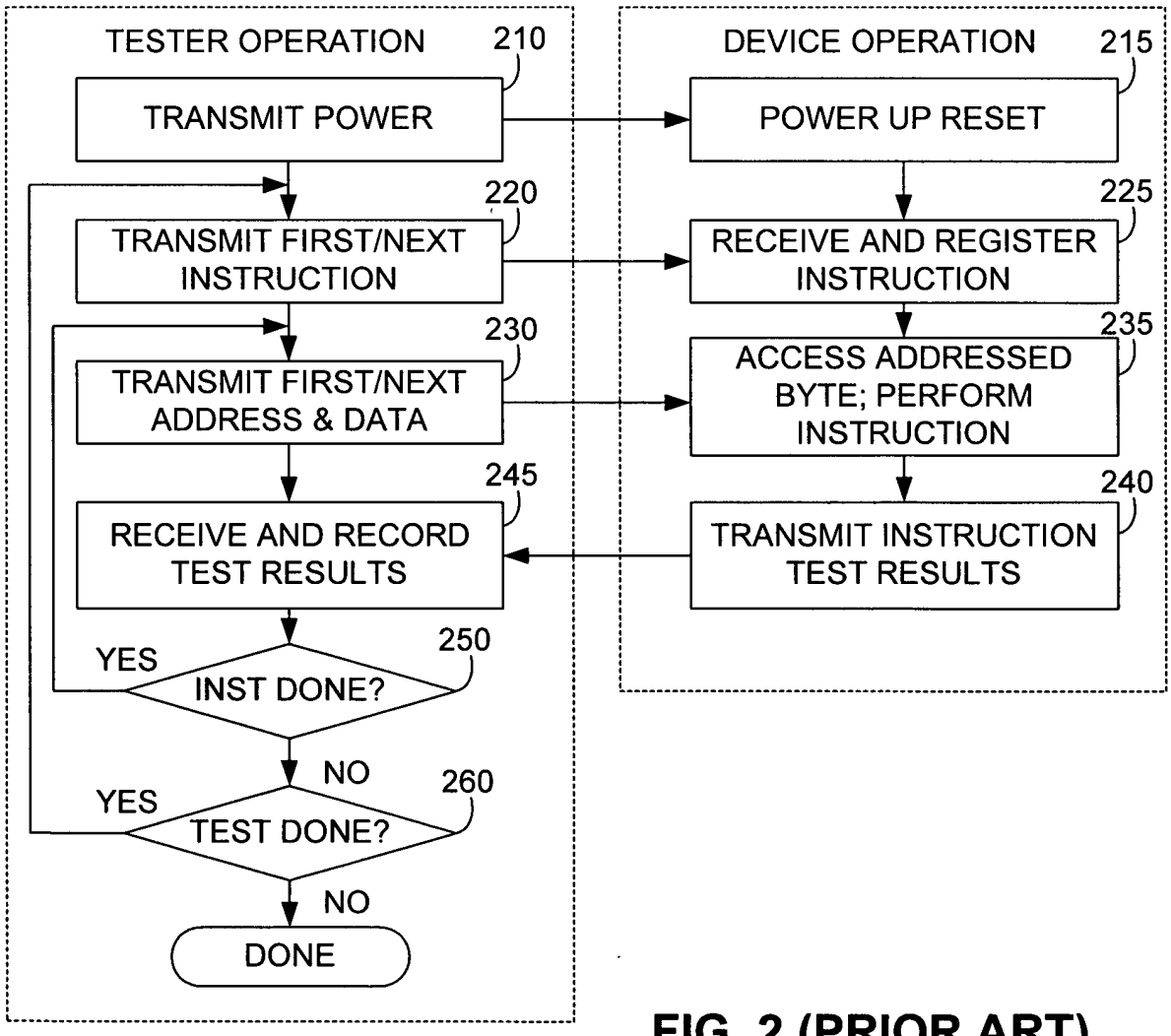

FIG. 2 (PRIOR ART)

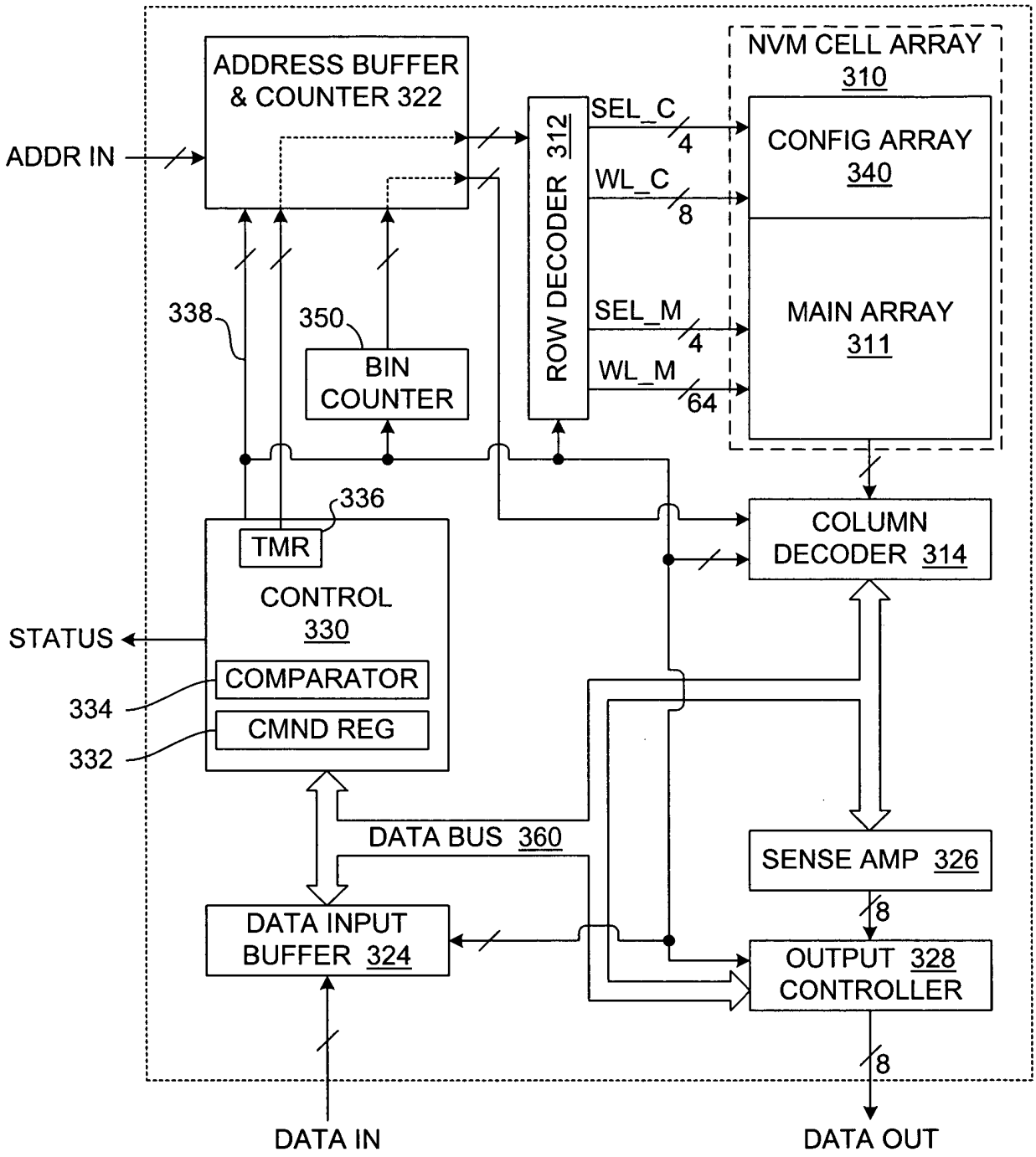
NVM CELL ARRAY
310
ADDRESS BUFFER
& COUNTER 322
ADDR IN
ROW DECODER 312
SEL_C
4
WL_C
8
CONFIG ARRAY
340
MAIN ARRAY
311
SEL_M
4
WL_M
64
338
350
BIN
COUNTER
336
TMR
CONTROL
330
COLUMN
DECODER 314
STATUS
COMPARATOR
CMND REG
334
332
DATA BUS 360
SENSE AMP 326
8
DATA INPUT
BUFFER 324
OUTPUT 328
CONTROLLER
8
DATA IN
DATA OUT

FIG. 3

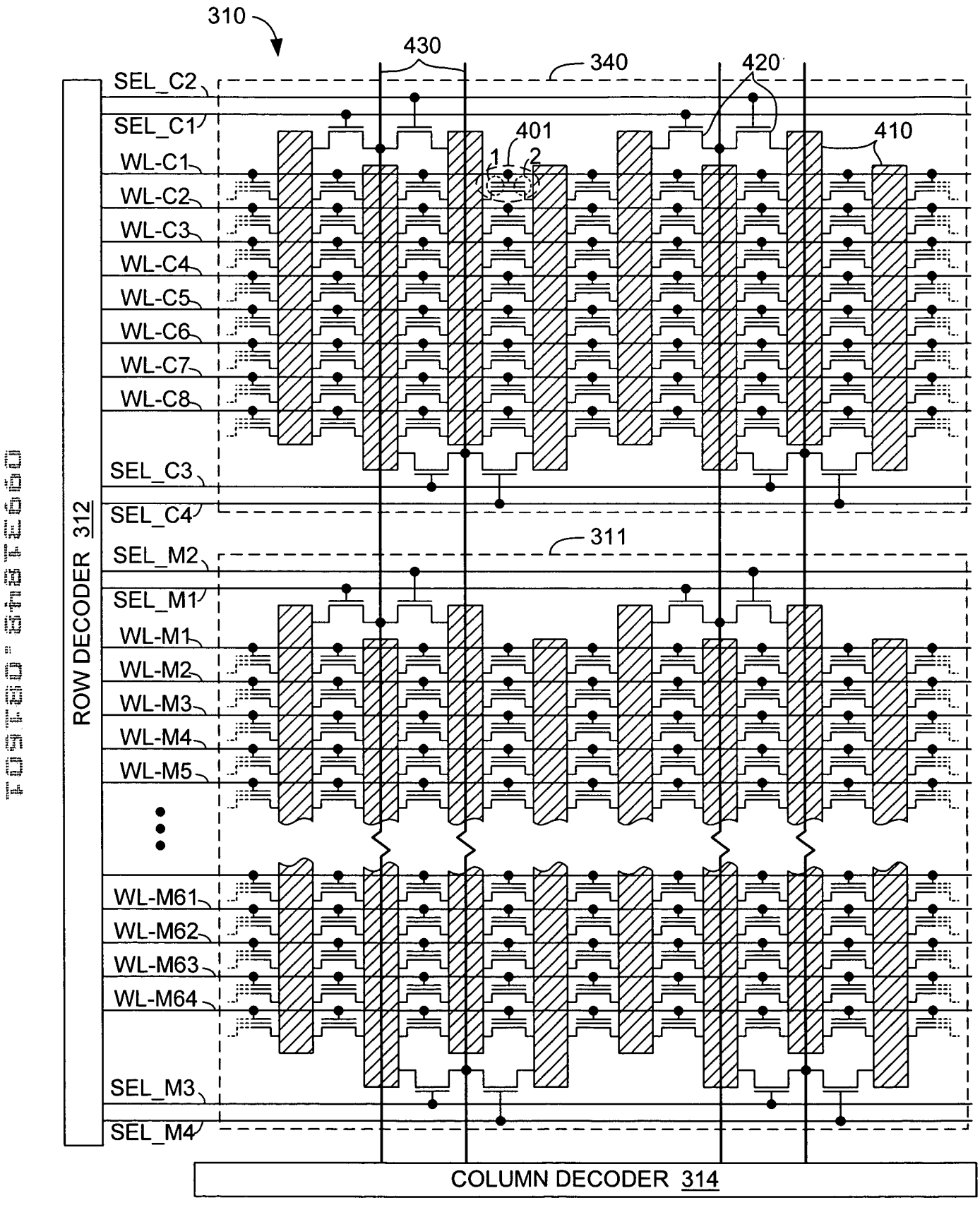
310
430
340
420
410
401
1
2
SEL_C2
SEL_C1
WL-C1
WL-C2
WL-C3
WL-C4
WL-C5
WL-C6
WL-C7
WL-C8
SEL_C3
SEL_C4
311
SEL_M2
SEL_M1
WL-M1
WL-M2
WL-M3
WL-M4
WL-M5
WL-M61
WL-M62
WL-M63
WL-M64
SEL_M3
SEL_M4
ROW DECODER 312
COLUMN DECODER 314

FIG. 4

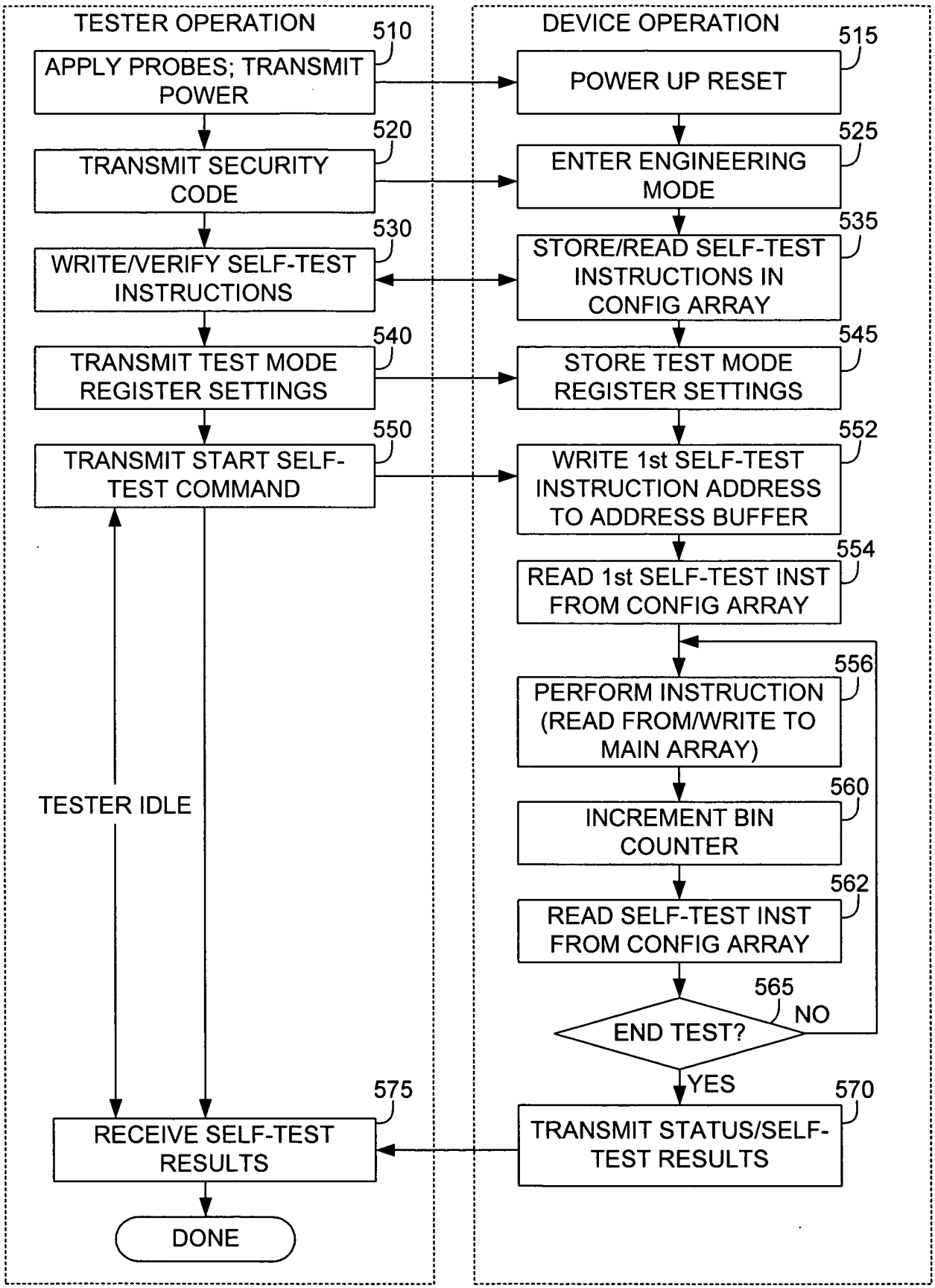
TESTER OPERATION
DEVICE OPERATION
510
APPLY PROBES; TRANSMIT POWER
515
POWER UP RESET
520
TRANSMIT SECURITY CODE
525
ENTER ENGINEERING MODE
530
WRITE/VERIFY SELF-TEST INSTRUCTIONS
535
STORE/READ SELF-TEST INSTRUCTIONS IN CONFIG ARRAY
540
TRANSMIT TEST MODE REGISTER SETTINGS
545
STORE TEST MODE REGISTER SETTINGS
550
TRANSMIT START SELF-TEST COMMAND
552
WRITE 1st SELF-TEST INSTRUCTION ADDRESS TO ADDRESS BUFFER
554
READ 1st SELF-TEST INST FROM CONFIG ARRAY
556
PERFORM INSTRUCTION (READ FROM/WRITE TO MAIN ARRAY)
560
INCREMENT BIN COUNTER
562
READ SELF-TEST INST FROM CONFIG ARRAY
565
END TEST?
NO
YES
TESTER IDLE
575
RECEIVE SELF-TEST RESULTS
570
TRANSMIT STATUS/SELF-TEST RESULTS
DONE

FIG. 5

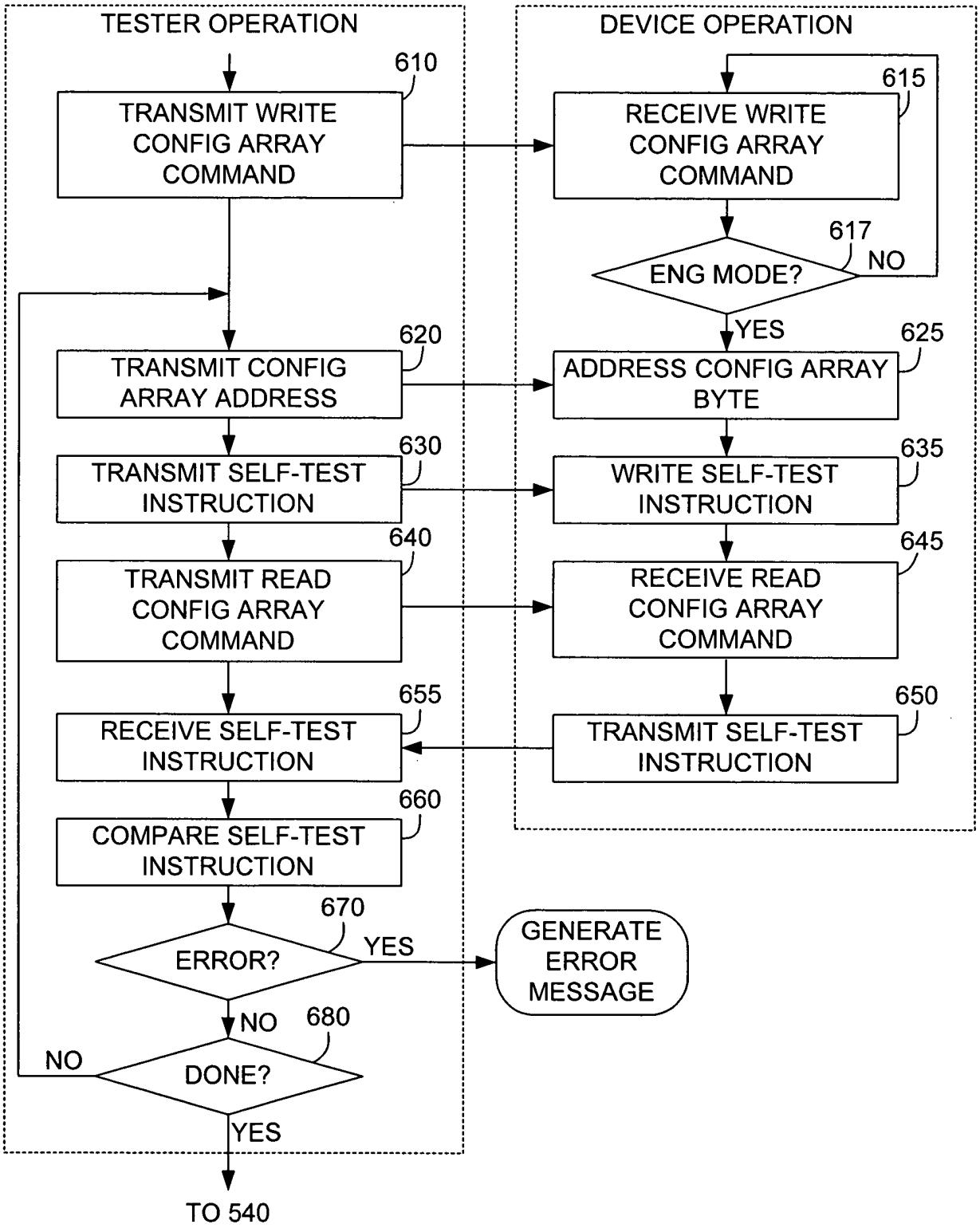
TESTER OPERATION
DEVICE OPERATION
610
TRANSMIT WRITE CONFIG ARRAY COMMAND
615
RECEIVE WRITE CONFIG ARRAY COMMAND
617
ENG MODE?
NO
YES
620
TRANSMIT CONFIG ARRAY ADDRESS
625
ADDRESS CONFIG ARRAY BYTE
630
TRANSMIT SELF-TEST INSTRUCTION
635
WRITE SELF-TEST INSTRUCTION
640
TRANSMIT READ CONFIG ARRAY COMMAND
645
RECEIVE READ CONFIG ARRAY COMMAND
655
RECEIVE SELF-TEST INSTRUCTION
650
TRANSMIT SELF-TEST INSTRUCTION
660
COMPARE SELF-TEST INSTRUCTION
670
ERROR?
YES
GENERATE ERROR MESSAGE
NO
680
NO
DONE?
YES
TO 540

FIG. 6

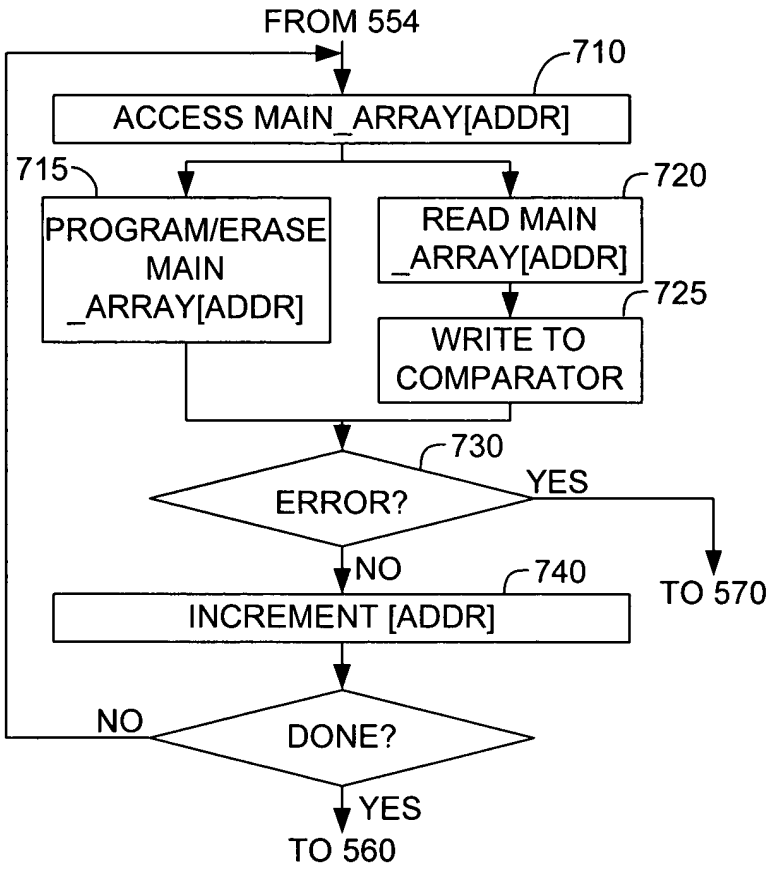

FIG. 7

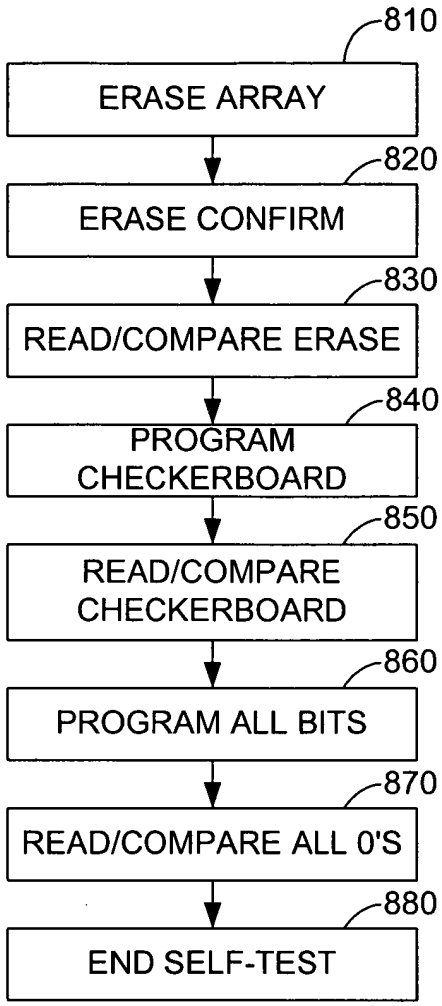

FIG. 8

BIT ADDR	0	0	1	1	2	2	3	3
BYTE 0/1	1	1	1	1	1	1	1	1
BYTE 2/3	1	1	1	1	1	1	1	1
BYTE 4/5	1	1	1	1	1	1	1	1
BYTE 6/7	1	1	1	1	1	1	1	1

FIG. 9(A)

BIT ADDR	0	0	1	1	2	2	3	3
BYTE 0/1	0	0	0	0	0	0	0	0
BYTE 2/3	0	0	0	0	0	0	0	0
BYTE 4/5	0	0	0	0	0	0	0	0
BYTE 6/7	0	0	0	0	0	0	0	0

FIG. 9(C)

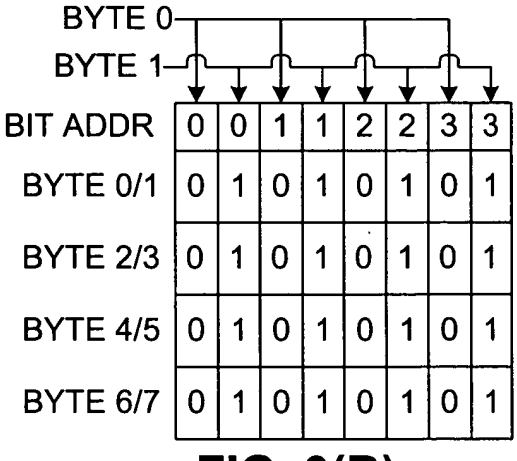

FIG. 9(B)